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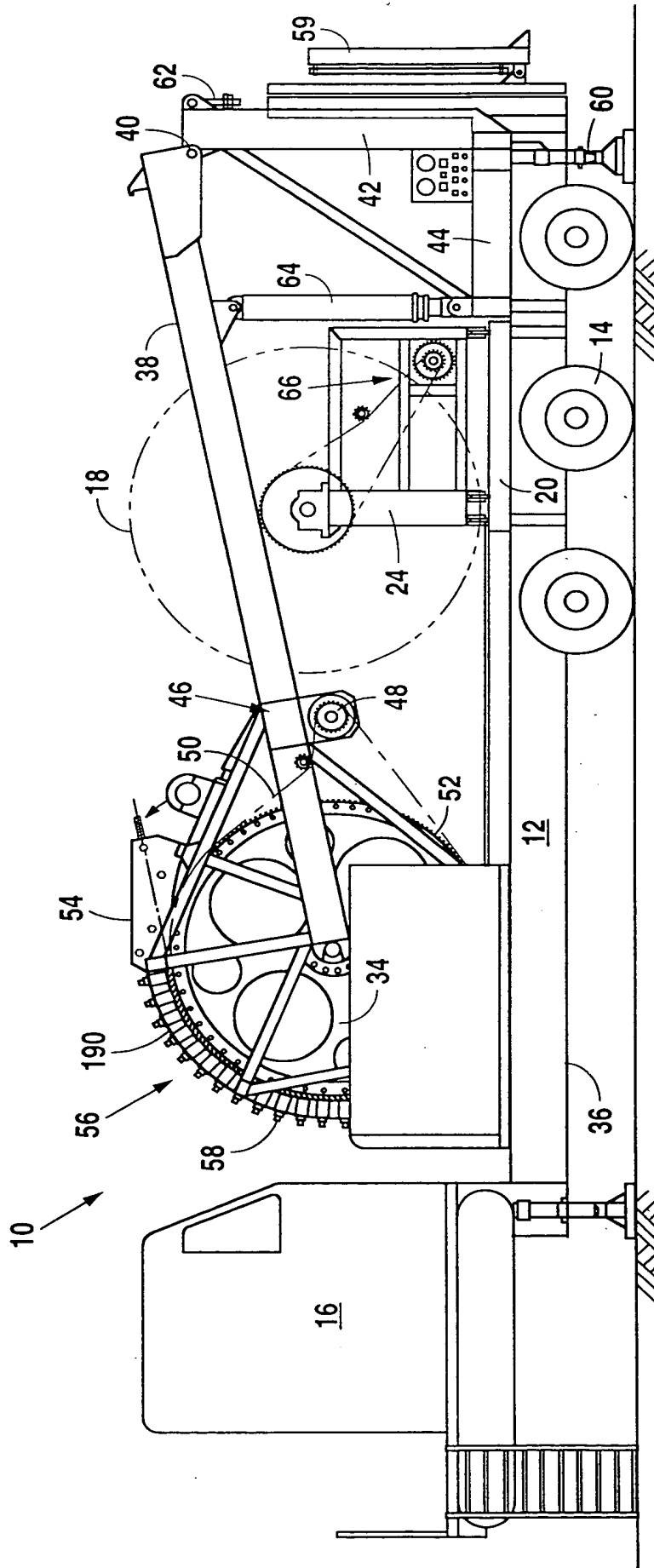


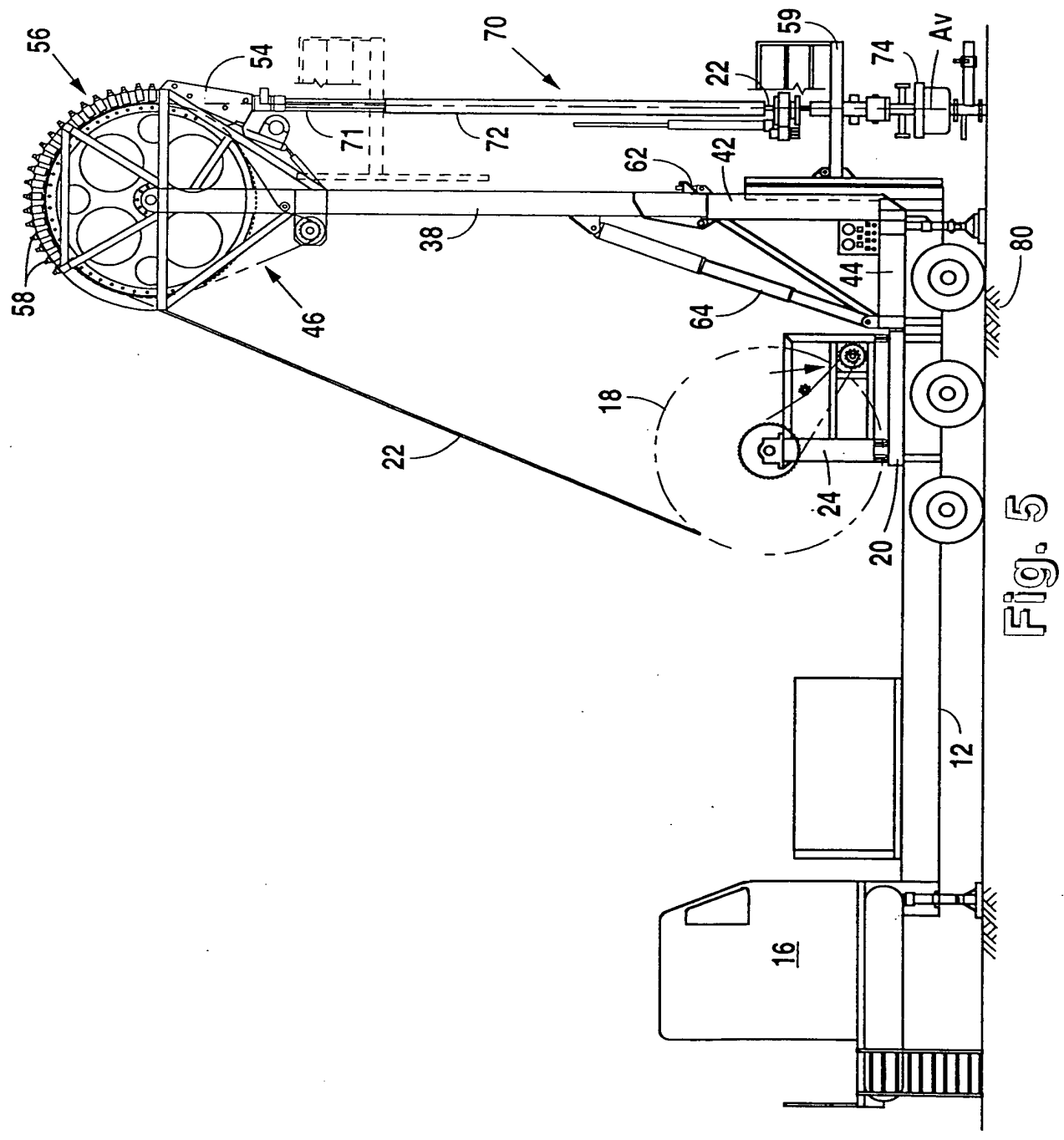
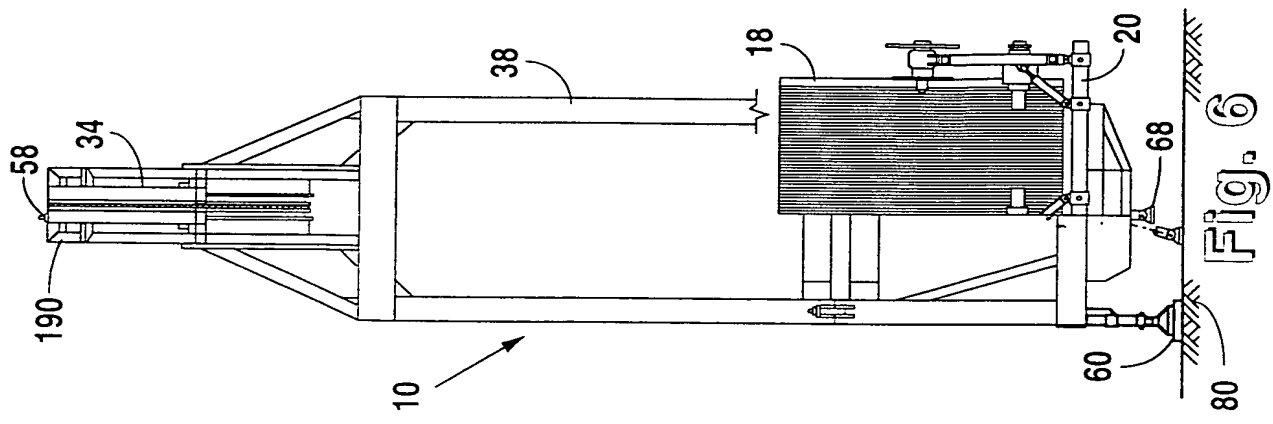
Fig. 1

The diagram illustrates a parallel plate capacitor. The top plate is a rectangle with a total length labeled A and a width labeled B . Below the top plate, a dielectric slab is shown, represented by a series of vertical lines. The height of this dielectric slab is labeled C , and its width is labeled D . The bottom plate is shown as a solid rectangle below the dielectric slab.

Fig. 4A
(PRIOR ART)

Fig. 4

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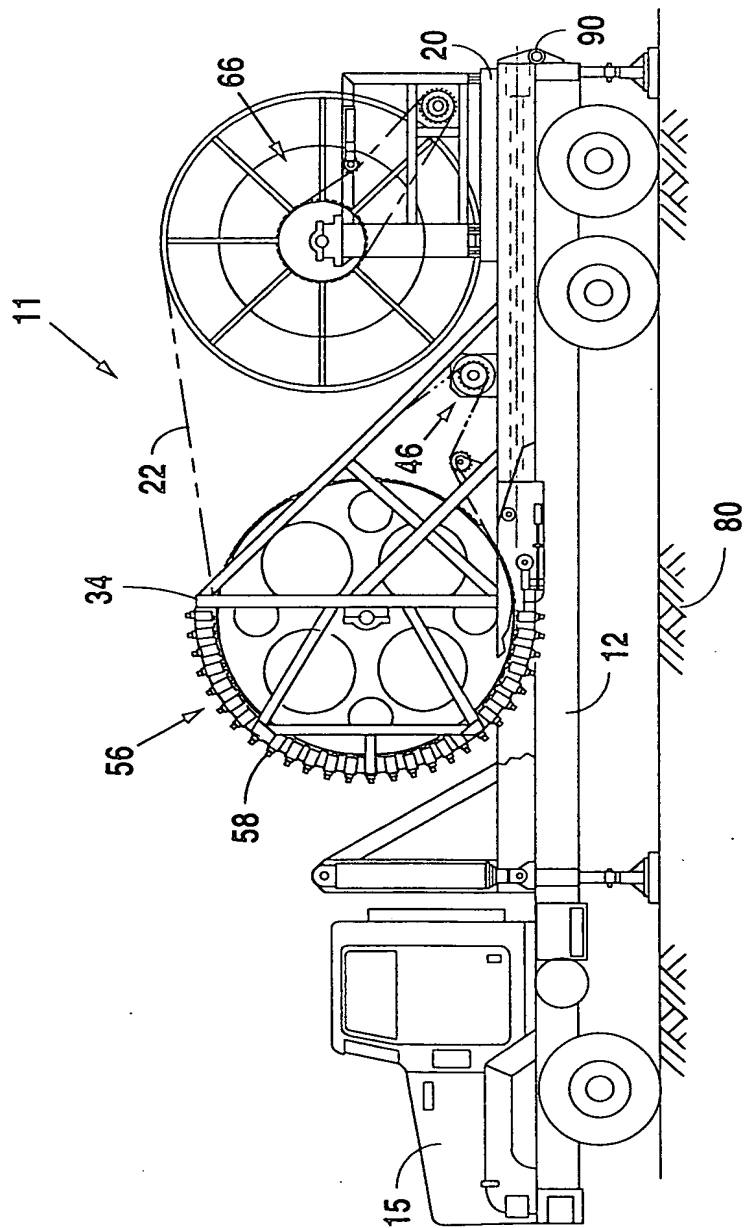


Fig. 7

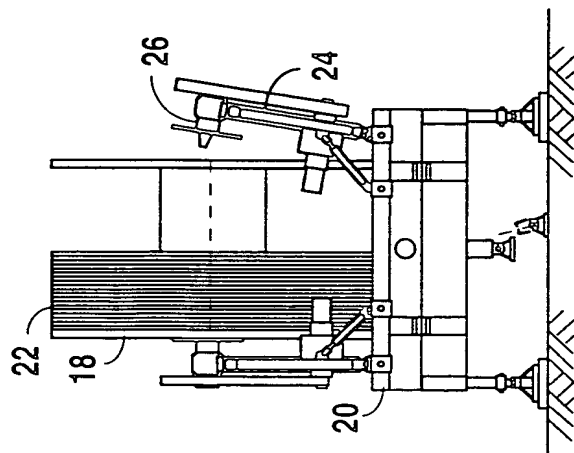


Fig. 8

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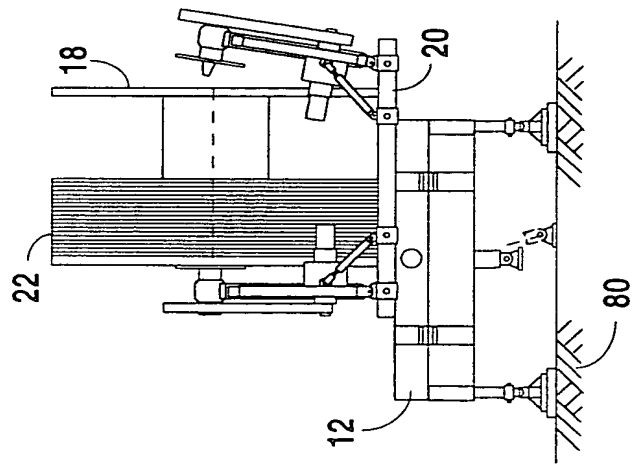


Fig. 10

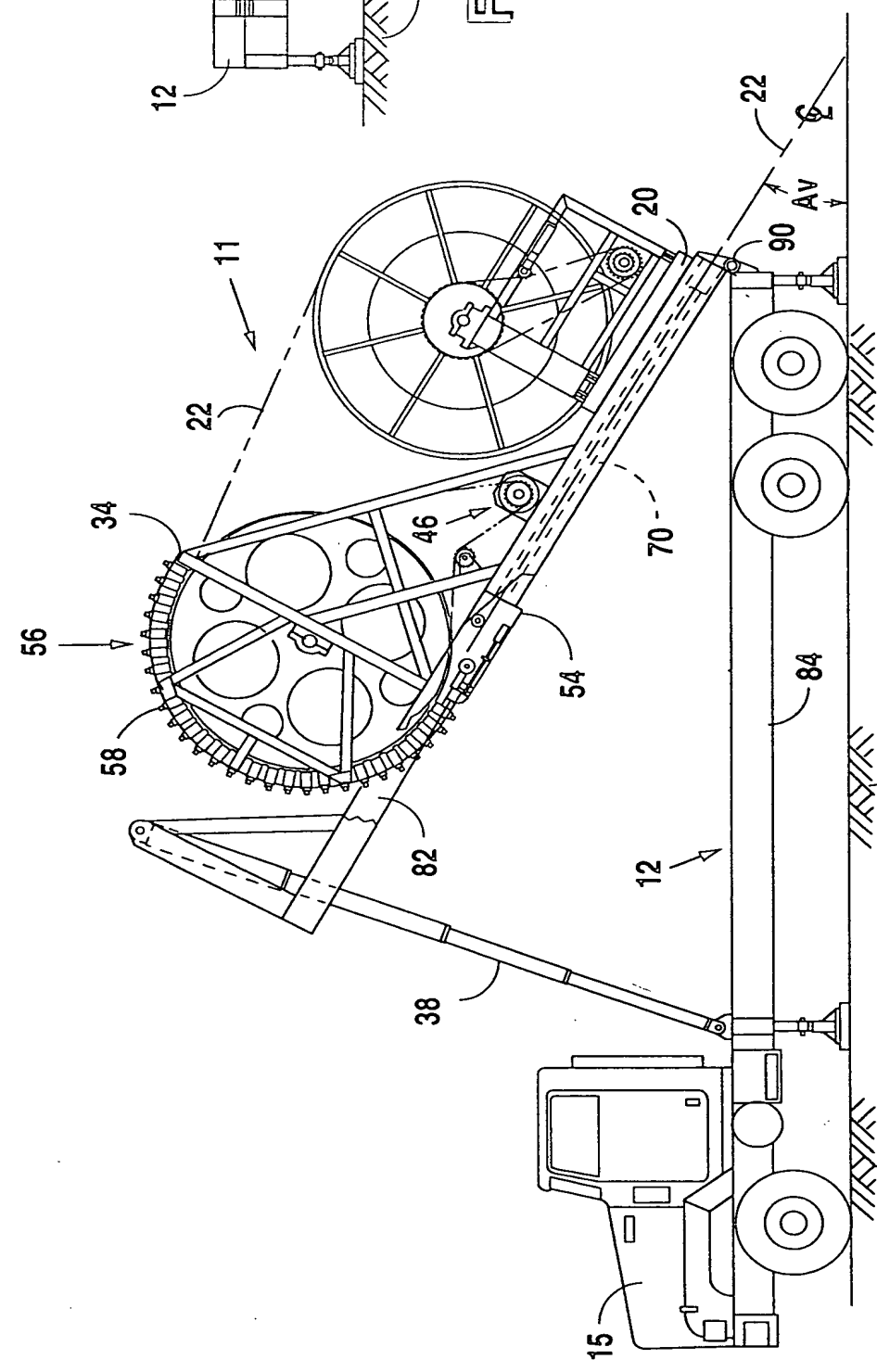


Fig. 9

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00484260 011800
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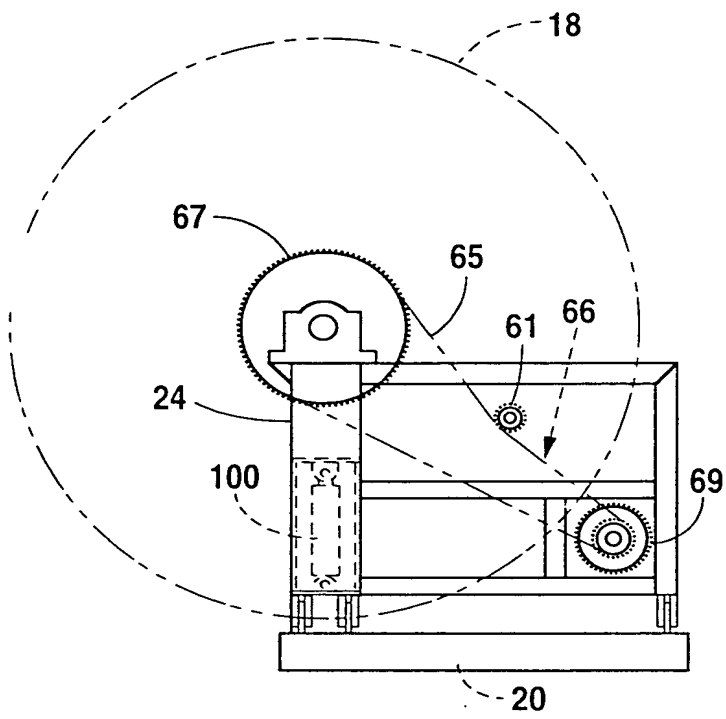


Fig. 11

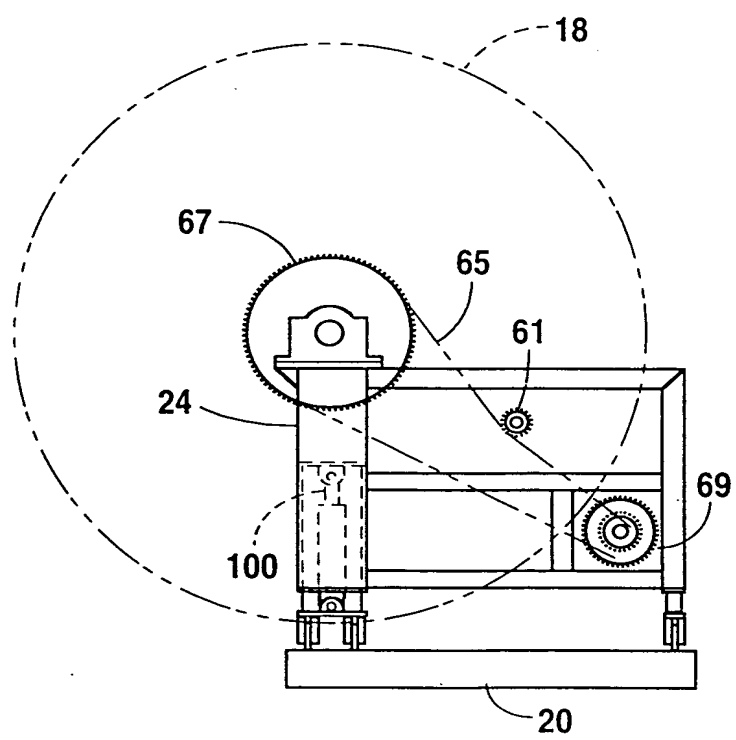


Fig. 12

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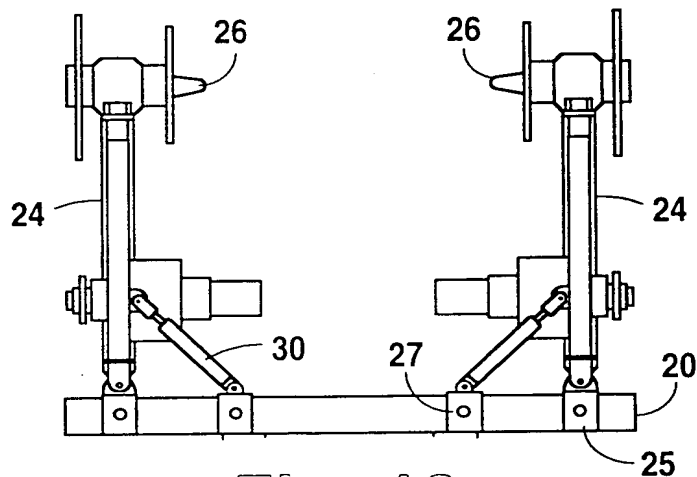


Fig. 13

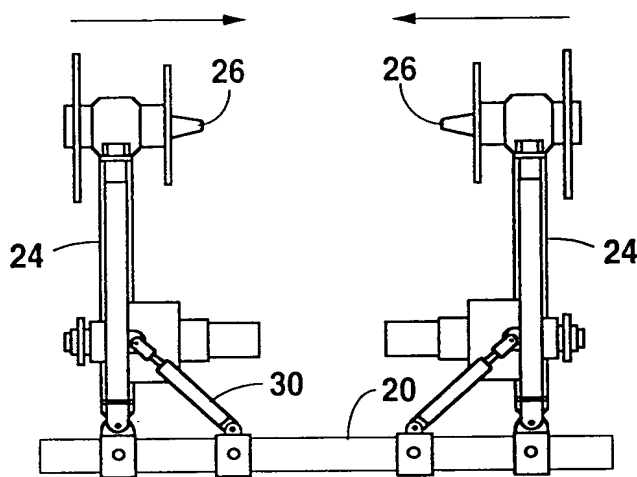


Fig. 14

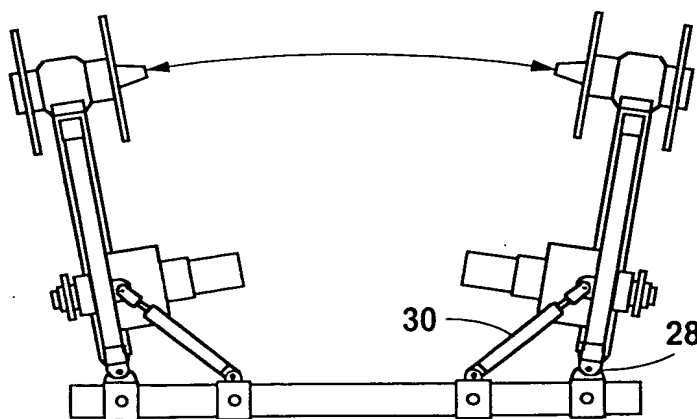


Fig. 15

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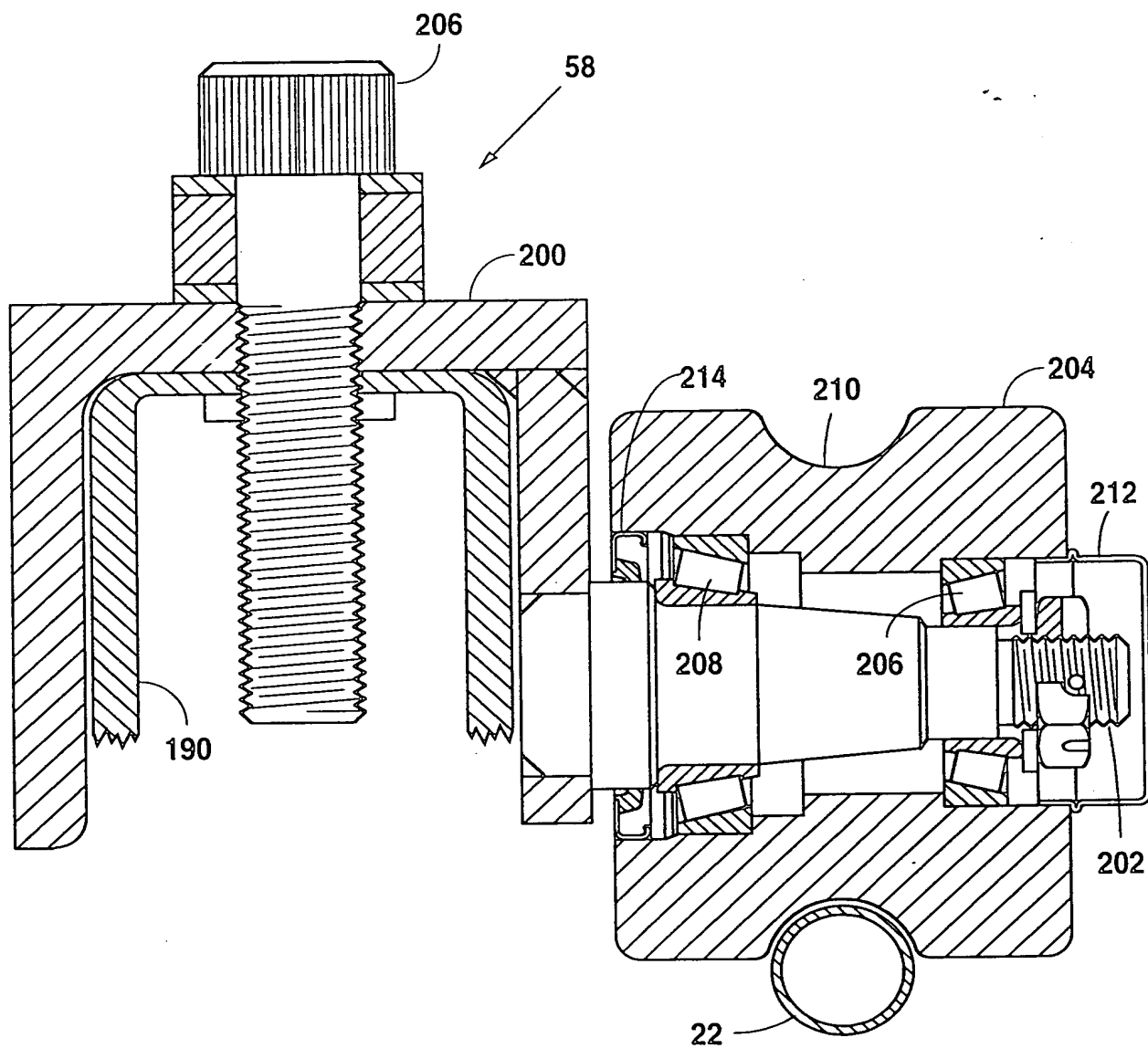


Fig. 16